IN THE CLAIMS:

1. (Currently Amended) A method for manufacturing a semiconductor device, comprising:

a first step of forming a gate electrode on a semiconductor region via a gate insulative film;

a second step of forming an amorphous layer in an upper portion of the semiconductor region by implanting ion of a group IV element into the semiconductor region using the gate electrode as a mask;

after the second step, a third step of implanting a first impurity of a first conductivity type into the semiconductor region in which the amorphous layer is formed using the gate electrode as a mask with an implantation projected range such that the first impurity reaches a position deeper than the amorphous layer; and

after the third step, a fourth step of subjecting the upper portion of the semiconductor region to thermal annealing so as to form a dislocation loop defect layer and an extension high concentration diffusion layer of the first conductivity type through diffusion of the first impurity, the extension high concentration diffusion layer having a junction at a position deeper than the ~~amorphous~~ dislocation loop defect layer.

2. (Original) The method for manufacturing a semiconductor device of claim 1, wherein:

the third step includes a step of implanting a second impurity of a second conductivity type into the semiconductor region using the gate electrode as a mask with an implantation projected range such that the second impurity reaches a position deeper than the amorphous layer; and

the fourth step includes a step of forming a pocket diffusion layer of the second conductivity type through diffusion of the second impurity under the extension high concentration diffusion layer.

3. (Currently Amended) The method for manufacturing a semiconductor device of claim 1, further comprising, after the fourth step:

a step of forming a side wall made of an insulative film on a side surface of the gate electrode; and

a step of implanting a third impurity of the first conductivity type into the semiconductor region using the gate electrode and the side wall as a mask, and then

performing thermal annealing, so as to form a high concentration diffusion layer of the first conductivity type through diffusion of the third impurity, the high concentration diffusion layer of the first conductivity type being located on an outer side of the extension high[[.]] concentration diffusion layer and having a junction plane at a position deeper than the extension high concentration diffusion layer.

4. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the group IV element is silicon or germanium.

5. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the second step includes implanting ion of the group IV element at a dose equal to or greater than a dose such that the semiconductor region is turned into an amorphous state.

6. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the third step includes implanting the second impurity with an implantation projected range of about 14 nm or less.

7. (Currently Amended) The method for manufacturing a semiconductor[[.]] device of claim 1, wherein the second impurity is a molecule containing boron fluoride or fluorine.

8. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the second impurity is boron.

9. (Original) The method for manufacturing a semiconductor device of claim 1, wherein the third step includes a step of performing a plurality of iterations of ion implantation of the first impurity each at a dose less than or equal to a dose such that the

semiconductor region is turned into an amorphous state, each of the iterations of ion implantation being followed by thermal annealing so as to restore a crystallinity of the semiconductor region.

10. (Original) The method for manufacturing a semiconductor device of claim 1, further comprising, between the first step and the third step, a step of forming an insulative film on the semiconductor region so as to cover an exposed portion of the semiconductor region.